What Is Claimed Is:

1. In an electrically programmable and erasable memory device having a substrate of semiconductor material of a first conductivity type and having a first and second spaced-apart regions formed in the substrate of a second conductivity type, with a non-co-planar channel region formed in the substrate therebetween, wherein said non-co-planar channel region having two portions: a first portion and a second portion, an electrically conductive control gate having a portion disposed adjacent to and insulated from the first portion of the channel region for creating an inversion layer therein, a floating gate having a portion disposed adjacent to and insulated from the second portion of the channel region by an insulator, for creating a depletion region having field lines directed to the floating gate, wherein said first region is adjacent to the inversion layer, a method of programming said device comprises:

creating said inversion layer;

generating a stream of electrons at said first region and causing said stream of electrons to traverse through said inversion layer; and

accelerating said stream of electrons through said depletion region by said field lines, with little or no scattering, causing said electrons to be accelerated through said insulator and injected onto the floating gate.

2. The method of claim 1 wherein said channel region has a first portion along a horizontal surface and a second portion in a trench.

3. The method of claim 1 wherein said channel region has a first portion in a trench and a second portion along a horizontal surface.

4. The method of claim 2 wherein said first portion is substantially perpendicular to the second portion.

5. The method of claim 4 wherein said inversion layer having a pinch off point, adjacent to or in said depletion region, and wherein said stream of electrons originates at said pinch off point for acceleration through said depletion region.